Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB; PLUR=YES; OP=OR			
L22	L21 same address	28	L22
L21	L20 same l19	78	L21
L20	memory adj1 cell	69516	L20
L19	L1 same redundan$	4254	L19
L18	L15 same cell	22	L18
L17	L15 same redundant	9	L17
L16	L15 same rom	11	L16
L15	L1 adj1 control	335	L15
L14	5986952[uref]	2	L14
L13	L2 and fuse	12	L13
L12	L7 and rom	2	L12
L11	l1 same address	4821	L11
L10	L7 same rom	0	L10
L9	L7 and l1	0	L9
L8	L7 same l3	0	L8
L7	fuse-controlled or (fuse adj1 controlled)	101	L7
L6	L3 same rom	7	L6
L5	L2 same address same fuse	0	L5
L4	L3 same l1	0	L4
L3	static adj1 address	209	L3
L2	L1 same rom	1419	L2
L1	(error adj1 correction) or error-correction	39863	L1

END OF SEARCH HISTORY

L22: Entry 14 of 28 File: USPT Jul 6, 1999

DOCUMENT-IDENTIFIER: US 5920512 A
TITLE: Dynamic address remapping decoder

Brief Summary Text (5):
Furthermore, several memory systems utilizing fail maps exist in the prior art. A programmable read only memory ("PROM") utilized to recognize the addresses of faulty memory locations to cause a redundant memory to be selected for data storage was described in Tsang (U.S. Pat. No. 4,376,300). A separate permanent memory used to record bad cells and devices for continuous reference to avoid access to defective cells was described in Anderson et al. (U.S. Pat. No. 4,493,075). A MAP identifying memory chips having faulty memory locations was used to connect data lines to a good location in a spare memory chip as disclosed in MacDonald (U.S. Pat. No. 5,406,565). Another memory system compares the address of a data signal to a stored address of a defective memory cell and, if they agree, redirects the data signal to a spare memory cell (Fujiwara, U.S. Pat. No. 5,475,648). These systems and methods are time consuming because the matching process must sort through relatively large fail maps to try and locate a matching map. Also, they are inaccurate because the faults generated when the DRAMS are on a SIMM will likely only show a portion of the failures that were detected in the DRAM fail maps generated prior to assembly on a SIMM. Moreover, should too many defective memory locations be present in the main memory devices, these prior art techniques may be susceptible to overcrowding the spare memory device(s), or overlapping a redirected data signal on a defective memory location in the spare memory. These problems lead to the need for more error correction algorithms, reduced memory capacity, and, consequently, reduced data transfer rates.

L13: Entry 6 of 12 File: USPT Nov 16, 1999

DOCUMENT-IDENTIFIER: US 5986952 A
TITLE: Redundancy concept for memory circuits having ROM memory cells

Brief Summary Text (6):
One possible way of providing redundancy in a ROM memory (Read Only Memory) is described in U.S. Pat. No. 5,388,075, which shows that defective ROM memory cells are replaced by redundant programmable ROM memory cells (PROM memory cells). The ROMs which, in the event of redundancy, are programmed by fuses in such a way that they subsequently contain the data to be stored in the memory cells to be replaced. The solution has the disadvantage that the redundant memory cells, in the form of PROM memory cells, are relatively large.

Brief Summary Text (17):
In accordance with an added feature of the invention, there is an addressable third unit having read-only memory cells for storing parity bits, the repair means determining the data to be stored originally in the ROM memory cells of the first units replaced by the at least one redundant second unit is accomplished by error correction codes using the parity bits.

Detailed Description Text (5):
In the read-only memory cells 13 of the third unit E3 it is possible to store parity bits, which serve for the reconstruction of the data content of defective cells of the ROM memory cells 11 by error correction codes in an extended initialization phase of the memory during its start-up, as will be explained further below. The initialization according to the invention is to be performed each time the memory is started up, since, as is known, RAM memory cells are volatile memories.

Detailed Description Text (34):
If, on the other hand, in the event of redundancy, in FIG. 3 the upper or lower unit of the first units E1 having modified memory cells 14 has been replaced by the second unit E2, then it is necessary for the repair device 5, with the assistance of error correction codes, to perform a reconstruction of the data content of the individual replaced ROM memory cells 11 and to store the reconstructed data in the RAM memory cells 12. In this case, it is possible to make use for example of the parity bits P in the read-only memory cells 13, as explained with regard to FIG. 1.

Detailed Description Text (35):
FIG. 4 shows a different exemplary embodiment of details of the memory in FIG. 1. The first units E1 and the second units E2 are, as in FIG. 1, "normal" word lines WL and redundant word lines WL', respectively. Word addresses WADR for the addressing of the normal word lines WL can be decoded by the normal word line decoder 20 and the corresponding word line WL can be selected in this way. At the same time, the word address WADR can be decoded by a redundancy word line decoder 20' (which is illustrated as one unit together with the word line decoder 20 in FIG. 1). If, in the event of redundancy, one of the first units E1 has been replaced by the second unit E2, the corresponding word address WADR is programmed in the redundancy word line decoder 20'. This is customarily done by fuses following the fabrication and testing of the memory. If the redundancy word line decoder 20' then responds to an applied word address WADR, it generates a redundancy activation signal REN, which leads, on the one hand, to deactivation of the normal word line decoder 20 and, on the other hand, to selection of the corresponding redundant word line WL'.

CLAIMS:

2. The memory circuit according to claim 1, including an addressable third unit having read-only memory cells for storing parity bits, said repair means determining said data

to be stored originally in said ROM memory cells of said first units replaced by said at least one redundant second unit is accomplished by error correction codes using said parity bits.

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L22: Entry 9 of 28 File: USPT Apr 17, 2001

DOCUMENT-IDENTIFIER: US 6219286 B1
TITLE: Semiconductor memory having reduced time for writing defective information

Brief Summary Text (19):
According to a 7th aspect of the present invention, the semiconductor memory of the 6th aspect comprises the redundancy information comprising the defect address and information for correcting errors in the defect address; and data decision means for subjecting the redundancy information which is read from the redundancy information block by the data reading means to the error correction, extracting the defect address, and outputting the defect address to the register unit. Therefore, the semiconductor memory which can normally replace defective memory cells with redundant memory cells even when the redundancy information block which is not subjected to the replacement has a defect and the redundancy information has an error can be provided.

Detailed Description Text (51):
FIG. 5 is a block diagram illustrating a semiconductor memory according to a third embodiment of the present invention. In this figure, the same reference numerals as those in FIG. 4 denote the same or corresponding parts. In FIG. 5, a memory cell array 51 comprises a redundancy information block RBLK and a memory 6 cell array block 50. The memory cell array block 50 has the same structure as that of the memory cell array 11 in the second embodiment. The redundancy information block RBLK comprises nonvolatile memory cells which are arranged like a matrix. The redundancy information block RBLK contain redundancy information which includes an encoded defect address indicating a defective word line. Considering a case where errors occur in data, it is desirable that the redundancy information stored in the redundancy information block RBLK should be redundancy information having a plurality of same defect addresses or redundancy information which is obtained by adding error correction codes for correcting errors to a defect address. A row decoder 2a is the row decoder 2 described in the second embodiment in which a row address is decoded, whereby a memory cell in the redundancy information block RBLK can be selected. A redundancy control circuit 13 replaces the defective memory cells in word lines with redundant memory cells in the memory cell array block 50. A register unit 54 has almost the same structure as that of the register unit 14 in the second embodiment. The register unit 54 is different from the register unit 14 in that the register unit 54 receives and thereafter holds the defect address which is read from the redundancy information block RBLK.

Detailed Description Text (60):
FIG. 6 is a block diagram illustrating a semiconductor memory according to a fourth embodiment of the present invention. In this figure, the same reference numerals as those in FIG. 5 denote the same or corresponding parts. A memory cell array 60 comprises plural nonvolatile memory cells which are arranged like a matrix. A part of the area in the memory cell array 60 is a redundancy information block RBLK which contains redundancy information including a defect address. The remaining data area consists of (1+2) erase blocks BLK1.about.BLK(1+2) (1: positive integer) arranged successively in units of erase blocks each being constituted by a prescribed number of (two or more) word lines which are arranged successively. Here, the redundancy information having a plurality of the same defect addresses or the redundancy information having an error correction code added thereto is recorded in the redundancy information block RBLK. A block decoder 21 decodes a block address in the input row address, and outputs a block selection signal for selecting the erase block and redundancy information block in the memory cell array 60 through output signal lines B0.about.Bl, respectively. The output signal lines B1.about.Bl are connected to the redundancy control circuit 3. The output signal line B0 is input to a row-in-block decoder 22, and used for selecting the redundancy information block RBLK. The redundancy control circuit 3 has a similar structure to that of the redundancy control circuit as described in the first embodiment. However, in this case, the n detect

address decoder cells, the (n+1) control cells and the (n+1) selection circuits are replaced with 1 defect address decoders, (1+1) control cells and (1+1) control circuits. In place of the n output signal lines from the row decoder, the output signal lines B1.about.Bl of the block decoder are connected to the redundancy control circuit. The (1+1) control circuits respectively control switching of the input signal lines from the row-in-block decoder, in place of the word lines. The row-in-block decoder 22 selects the word line in accordance with the block selection signal and address which are output through the redundancy control circuit 3. A register unit 64 has almost the same structure as that of the register unit in the first embodiment. The register unit 64 is different from the register unit in the first embodiment in that the register unit 64 holds the defect address which is read from the redundancy information block RBLK, like the register unit as described in the third embodiment. A power-on detection circuit 8 detects that the semiconductor memory itself is powered on, and outputs an operation start signal to a data reading control circuit 6. The data reading control circuit 6 receives the operation start signal, and starts control for replacing the defective memory cell with the redundant memory cell.

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L13: Entry 11 of 12 File: USPT Aug 25, 1987

DOCUMENT-IDENTIFIER: US 4689792 A
TITLE: Self test semiconductor memory with error correction capability

Brief Summary Text (7):
To increase yield in a semiconductor memory array, such techniques as redundancy and error detection/correction schemes have been utilized. Redundancy is especially suited for repetitive circuits such as memory arrays wherein a portion of the circuits such as a column of memory cells is repeated on the chip. At test, it is then only necessary to either open a laser type fuse to insert the redundant circuit for the defective circuit or activate an electronic switching interface to make the replacement. One type of redundant circuit is discussed in patent application Ser. No. 693,417, (now U.S. Pat. No. 4,598,388) assigned to Texas Instruments Incorporated. Another device is disclosed in U.S. Pat. No. 4,471,472, issued to E. S. Young on Sept. 11, 1984 and assigned to Advanced Microdevices, Inc. Redundant circuits, however, require a defined amount of silicon surface area or "overhead" for implementation thereof. In addition, redundant circuits must be activated during the manufacturing phase with the redundancy provided therefor constrained within the limits of the redundant circuit. Partial redundancy works well only with Read/Write memories. Read Only Memories (ROM's) need 100% redundancy.

Detailed Description Text (11):
The block code error detect circuit 30 in the preferred embodiment utilizes a Hamming single error detecting and correcting code. However, it should be understood that some other suitable block code such as a Reed-Muller or Golay code could be utilized. The error correction code on the bus 32 contains information regarding the error in the form of the relative position within the 32 bit collective data word accessed and output on data bus 26. It is then only necessary to invert the bit in error to output a correct data word. The error correction circuit 34 facilitates this correction and the data word select circuit 37 selects a smaller segment data word for output on a bus 45 in accordance with the output select portion of the column address on bus 20. In this manner, a sixteen bit data word, an eight bit data word or a four bit data word can be output with the error correction being performed on a 32 bit data word. This results in a smaller number of parity bits to perform the error correction. For example, a 32 bit word would require only six parity bits whereas four eight bit data words would require four parity bits each for a total of sixteen parity bits. Further, fewer accesses need to be made to self test the ROM since each access cycle selects four data words.

Detailed Description Text (39):
In summary, there has been provided a self testing ROM which requires accessing of the data in two passes. In the first pass, the data is accessed and input to an error detect/correct circuit for correction of the data. The correct data is then reinput to the error detect/correct circuit to determine if an error still exists. If an error exists, then too many errors existed in the initial accessed data word for correction by the error correction code utilized in the error detect/correct circuit. This error during the second pass is detected and a signal output to indicate that there is an error. To test an entire array, it is only necessary to step therough each of the memory locations and perform the self test on the accessed information. This alleviates the need to compare output data with a manufacturer's program to determine if the memory is good.

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L18: Entry 14 of 22 File: USPT May 4, 1999

DOCUMENT-IDENTIFIER: US 5901152 A
TITLE: Three-value data storing semiconductor memory system

Brief Summary Text (22):
According to the invention, there is provided still another type of a three-value data storing semiconductor memory system, which comprises: a memory cell array having a memory section which comprises a plurality of memory cells capable of storing a three-value data item and arranged in rows and columns, for storing data signals and check signals; and a error-correction control circuit for generating check binary data items from a plurality of binary data items to be stored in the memory cells, for detecting whether any binary data item read from the memory section is erroneous in accordance with the binary data items and the check binary data items, and for correcting any binary data that has been found to be erroneous, wherein the error-correction control circuit decomposes a plurality of binary data items to be stored in the memory cells to a plurality of symbols in a unit of three times bit length, generates a plurality of check binary data items to be stored in the memory cells, and detects and corrects data items in a unit of the symbols according to the binary data items and the check binary data items read from the memory cells.

Detailed Description Text (41):
The three-value data storing semiconductor memory system according to the present invention comprises, among other components, memory cell arrays and an error-correction control circuit. Each memory cell array has a memory section which has memory cells, which can store three-value data, arranged in rows and columns, for storing data signals and check signals. The error-correction control circuit is designed to generate check binary data items from the binary data stored in the memory cells, to detect whether each binary data item is erroneous or not, and to correct an erroneous binary data item, if any, in accordance with the check binary data item associated with the erroneous binary data item. To be more specific, the error-correction control circuit (i.e., the card control circuit 3 in the system of FIG. 1) decomposes the binary data stored in the memory cells, into symbols each consisting of 3k bits (k is 1, 2, 3, . . .) symbols and stored in the memory cells. The error-correction control circuit determines whether the symbols are erroneous or not, and corrects any erroneous symbol found, in accordance with the associated check binary data item.

CLAIMS:

15. A three-value data storing semiconductor memory system comprising:

a memory cell array having a memory section which comprises a plurality of memory cells capable of storing a three-value data item and arranged in rows and columns, for storing data signals and check signals; and

a error-correction control circuit for generating check binary data items from a plurality of binary data items to be stored in said memory cells, for detecting whether any binary data item read from said memory section is erroneous in accordance with the binary data items and the check binary data items, and for correcting any binary data that has been found to be erroneous,

wherein said error-correction control circuit decomposes a plurality of binary data items to be stored in said memory cells to a plurality of symbols in a unit of three times bit length, generates a plurality of check binary data items to be stored in said memory cells, and detects and corrects data items in a unit of said symbols according to the binary data items and the check binary data items read from said memory cells.

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End of Result Set

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L12: Entry 2 of 2 File: USPT Jan 8, 1991

DOCUMENT-IDENTIFIER: US 4984054 A
TITLE: Electric fuse for a redundancy circuit

Brief Summary Text (27):
Briefly described, the present invention comprises an electric fuse for a redundancy circuit comprising: a semiconductor substrate, a first insulating film formed on the surface of the semiconductor substrate, an underlying film formed on the surface of the first insulating film, a second insulating film formed on the surface of the first insulating film and the surface of the underlying film, with a surface stepped portion formed with the surface of the underlying film, and a fuse material formed along an edge of the underlying film on the surface stepped portion. Since a fuse material is formed along an edge of the underlying film on the surface stepped portion, the width of the blow out portion of an electric fuse in accordance with the present invention is controlled to be narrow.

Detailed Description Text (16):
In the above embodiment, although an electric fuse for a redundancy circuit MOS dynamic RAM was shown, the present invention can be applied to an electric fuse for a redundancy circuit of other semiconductor memories such as a MOS static RAM and ROM.

Detailed Description Text (18):
A bipolar PROM is a non-volatile read-only memory to which users can write a memory content electrically, which has a small memory capacity and has a large application as compared with EPROM (Erasable Programmable ROM). Memory cells consist of two kinds, that is, one is a fuse type having a blowout portion which is blown out by applying a current, and the other is a junction type shorting a junction by applying a reverse current to the emitter-base junction. The most significant feature of the bipolar PROM is that cells which have been once written are never reprogrammable. The present invention also can be applied to the above-mentioned fuse type bipolar PROM.